* NOTICES *



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CLAIMS

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[Claim(s)]
[Claim 1] It has the 1st semi-conductor layer of the 1st conductivity type which has the 1st principal plane and the 2nd principal plane, and the 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer. The 1st semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which said 1st semi-conductor layer has heights alternatively formed on said 2nd principal plane, and was formed in top face of said heights / semi-conductor ], Said heights of said 1st semi-conductor layer, and the 1st insulator layer of said 1st semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in said heights which counter said one side side, and the other side side of said 1st semiconductor region, The 2nd semiconductor region of the 2nd control electrode formed on said 2nd insulator layer, and the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 1st insulator layer, The 3rd semiconductor region of the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 2nd insulator layer, The semiconductor device further equipped with the 1st main electrode which became independent of said 1st and 2nd control electrodes, and was formed in contact with said 1st, 2nd, and 3rd semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer.
[Claim 2] It has the 1st semi-conductor layer of the 1st conductivity type which has the 1st principal plane and the 2nd principal plane, and the 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer. The 1st semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which has heights alternatively formed on said 2nd principal plane of said 1st semi-conductor layer, and was formed in top face of said heights / semi-conductor ], Said heights of said 1st semi-conductor layer, and the 1st insulator layer of said 1st semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in said heights which counter said one side side, and the other side side of said 1st semiconductor region, So that the 2nd control electrode formed on said 2nd insulator layer may be touched at said 1st and 2nd insulator layers both The 2nd semiconductor region of the 2nd conductivity type which consists of a discrete field where the plurality which was alternatively formed in said 1st semiconductor region front face, and was located in a line along with these 1st and 2nd insulator layers became independent, The semiconductor device further equipped with the 1st main electrode which became independent of said 1st and 2nd control electrodes, and was formed in contact with said 1st and 2nd semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer.
[Claim 3] The 1st semi-conductor layer of the 1st conductivity type which has the 1st principal plane and the 2nd principal plane, and the 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer, The 1st semiconductor region of the 2nd conductivity type alternatively formed on said 2nd principal plane of said 1st semi-conductor layer, The 2nd semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which was

alternatively formed in front face of said 1st semiconductor region / semi-conductor ], The 1st insulator layer of said 1st semiconductor region and said 2nd semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in the other side side of said 1st and 2nd semiconductor regions which counter said one side side, The 3rd semiconductor region of the 2nd control electrode formed on said 2nd insulator layer, and the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 1st insulator layer, The 4th semiconductor region of the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 2nd insulator layer, The semiconductor device equipped with the 1st main electrode which became independent of said 1st and 2nd control electrodes, and was formed in contact with said 2nd, 3rd, and 4th semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer.

[Claim 4] The 1st semi-conductor layer of the 1st conductivity type which has the 1st principal plane and the 2nd principal plane, and the 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer, The 1st semiconductor region of the 2nd conductivity type alternatively formed on said 2nd principal plane of said 1st semi-conductor layer, The 2nd semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which was alternatively formed in said 1st semiconductor region front face / semi-conductor ], The 1st insulator layer of said 1st semiconductor region and said 2nd semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in the other side side of said 1st and 2nd semiconductor regions which counter said one side side, So that the 2nd control electrode formed on said 2nd insulator layer may be touched at said 1st and 2nd insulator layers both The 3rd semiconductor region of the 2nd conductivity type which consists of a discrete field where the plurality which was alternatively formed in said 1st semiconductor region front face, and was located in a line along with these 1st and 2nd insulator layers became independent, The semiconductor device equipped with the 1st main electrode which became independent of said 1st and 2nd control electrodes, and was formed in contact with said 2nd and 3rd semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer.

[Claim 5] (a) The process which forms the 2nd semi-conductor layer of the 2nd conductivity type on said 1st principal plane of the 1st semi-conductor layer of the 1st conductivity type which has the 1st principal plane and the 2nd principal plane, (b) The process which forms heights alternatively on said 2nd principal plane of said 1st semi-conductor layer, (c) -- the top face of said heights of said 1st semi-conductor layer -- this -- with the process which forms alternatively the 1st semiconductor region of the 1st conductivity type of low resistance from the 1st semi-conductor layer (d) Said heights of said 1st semi-conductor layer, and the process of said 1st semiconductor region which forms the 1st insulator layer in a side face on the other hand, (e) The process which forms the 1st control electrode on said 1st insulator layer, and the process which forms the 2nd insulator layer in said heights which counter the (f) aforementioned one side side, and the other side side of said 1st semiconductor region, (g) The process which forms the 2nd control electrode on said 2nd insulator layer, and the process which forms the 2nd semiconductor region of the 2nd conductivity type in the front face of the 1st semiconductor region of (h) above alternatively in contact with said 1st insulator layer, (i) The process which forms the 3rd semiconductor region of the 2nd conductivity type in the front face of said 1st semiconductor region alternatively in contact with said 2nd insulator layer, (j) The manufacture approach of the semiconductor device equipped with the process which forms the 1st main electrode which became independent of said 1st and 2nd control electrodes, and touched said 1st, 2nd, and 3rd semiconductor regions, and the process which forms the 2nd main electrode which touched the semi-conductor layer of the (k) above 2nd.

[Claim 6] said process (c), and said said process (h) and said process (i) -- said 2nd principal plane of said 1st semi-conductor layer -- alternative -- the impurity of the 1st conductivity type -- being spread -- this -- with the process which forms said 1st semiconductor region of low resistance from the 1st semi-conductor layer [ a process (b), and ] The process which diffuses the impurity of the 2nd conductivity type alternatively on the front face of this 1st semiconductor region, and forms said 2nd and 3rd

semiconductor regions in coincidence, It has the process which forms the slot on the pair so that the 1st semi-conductor layer may become convex. a part of said 1st, 2nd, and 3rd semiconductor region and said 1st semi-conductor layer -- alternative -- coincidence -- etching -- these 1st, 2nd, and 3rd semiconductor regions -- this -- It has the process at which said process (d) and said process (f) form said 1st and 2nd insulator layers in coincidence by forming an insulator layer in the front face of the slot of said pair. The manufacture approach of the semiconductor device [ equipped with the process which forms said 1st and 2nd control electrodes in coincidence when said process (e) and said process (g) form a conductor in Mizouchi of said pair in which said insulator layer was formed ] according to claim 5.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the technique for improving especially the operating characteristic of that semiconductor device about the semiconductor device which operates with the electrical potential difference of a control electrode.
[0002]
[Description of the Prior Art] The top view and drawing 31 which show the structure of the semiconductor device of the former [ drawing 30 ] are the strabism sectional view showing the structure of the conventional semiconductor device. Drawing 31 is X-X strabismus sectional view in drawing 30 , and it has excluded the parts of a control electrode etc. in order to make cross-section structure intelligible. Setting to drawing 30 and drawing 31 , 1 is n. - An epitaxial layer and 2 are p+. Substrate, 3 is n. - The heights formed in the front face of an epitaxial layer 1 and 4 are n. - n+ formed in the top face of the heights 3 formed in the front face of an epitaxial layer 1 Diffusion field, 5 is heights 3 and n+. The insulator layer formed in the side face of the diffusion field 4 and 6 are heights 3 and n+. The control electrode of the pair formed on the insulator layer 5 across the diffusion field 4, 7 is n+. n of the trailer of the diffusion field 4 - p+ formed in the epitaxial layer 1 Diffusion field, 8 is p+. A part of diffusion field and n+ The insulator layer formed on a part of diffusion field 4 and the control electrode 6, 9 is n+. The diffusion field 4 and p+ The aluminum-Si electrode with which it is formed so that the diffusion field 7 may be contacted, and other parts are separated by the insulator layer 8, and 10 are p+. It is a metal electrode in contact with a substrate 2.
[0003] Next, actuation of this semiconductor device is explained using drawing 32 thru/or drawing 34 . n which is between control electrodes 6 when the potential of the control electrode 6 to an electrode 9 is lowered in drawing 32 , where the potential of the electrode 10 to an electrode 9 is raised - When the depletion layer extended from a control electrode 6 touches the heights 3 of an epitaxial layer 1 mutually, a potential barrier arises. Therefore, an electron will not flow toward an electrode 10 from an electrode 9. Thus, it can change into a current inhibition condition.
[0004] Next, if the potential of the control electrode 6 to an electrode 9 is raised, said potential barrier will disappear and an electron 12 will begin to flow toward an electrode 10 from an electrode 9. It is p+ to this and coincidence. A hole 11 is poured in from a substrate 2 and it is n. - Conductivity modulation is started by the epitaxial layer 1. The hole 11 poured in as shown in drawing 33 is n. - An epitaxial layer 1 or n+ It re-joins in the diffusion field 4, or is p+. It is absorbed by the diffusion field 7. Thus, a semiconductor device can carry out a turn-on.
[0005] Next, if the potential of the control electrode 6 to an electrode 9 is lowered again, a potential barrier will arise again in the heights 3 between control electrodes 6, and the electron current will not flow toward an electrode 10 from an electrode 9. And as shown in drawing 34 , as the hole 11 poured into coincidence at this time is accumulated in the front face of an insulator layer 5, it is transmitted to a surface part, and it is p+. Commutation is carried out to the diffusion field 7. Thus, the turn-off of the semiconductor device can be carried out.

[0006]
[Problem(s) to be Solved by the Invention] Since it is constituted as mentioned above, it is going to decrease ON state voltage, and the conventional semiconductor device is p+. n+ to the diffusion field 7 If area of the diffusion field 4 is enlarged, the commutation of the hole 11 at the time of a turn-off will take time amount, and the fall of switching speed and increase of a switching loss will be brought about.
[0007] On the contrary, p+ n+ to the diffusion field 7 Many of holes poured in by the ON state although switching speed and a switching loss have improved when area of the diffusion field 4 was made small are p+. It is n+ in order to commutate to the diffusion field 7. About four diffusion field n - An epitaxial layer 1 stops receiving sufficient conductivity modulation, and brings about the rise of ON state voltage.

[0008] Thus, in the conventional semiconductor device, ON state voltage, switching speed, and a switching loss had the relation of a trade-off, and there was a trouble that it was difficult to improve both to coincidence.
[0009] It was made in order that this invention might solve the above troubles, and ON state voltage is low, switching speed is quick, and it aims at a switching loss obtaining a small semiconductor device.
[0010]
[Means for Solving the Problem] The 1st semi-conductor layer of the 1st conductivity type with which the semiconductor device concerning the 1st invention has the 1st principal plane and the 2nd principal plane, It has the 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer. The 1st semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which said 1st semi-conductor layer has heights alternatively formed on said 2nd principal plane, and was formed in top face of said heights / semi-conductor ], Said heights of said 1st semi-conductor layer, and the 1st insulator layer of said 1st semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in said heights which counter said one side side, and the other side side of said 1st semiconductor region, The 2nd semiconductor region of the 2nd control electrode formed on said 2nd insulator layer, and the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 1st insulator layer, The 3rd semiconductor region of the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 2nd insulator layer, With said 1st and 2nd control electrodes, it becomes independent, and it has further the 1st main electrode formed in contact with said 1st, 2nd, and 3rd semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer, and is constituted.
[0011] Moreover, the 1st semi-conductor layer of the 1st conductivity type with which the semiconductor device concerning the 2nd invention has the 1st principal plane and the 2nd principal plane, It has the 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer. The 1st semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which has heights alternatively formed on said 2nd principal plane of said 1st semi-conductor layer, and was formed in top face of said heights / semi-conductor ], Said heights of said 1st semi-conductor layer, and the 1st insulator layer of said 1st semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in said heights which counter said one side side, and the other side side of said 1st semiconductor region, So that the 2nd control electrode formed on said 2nd insulator layer may be touched at said 1st and 2nd insulator layers both The 2nd semiconductor region of the 2nd conductivity type which consists of a discrete field where the plurality which was alternatively formed in said 1st semiconductor region front face, and was located in a line along with these 1st and 2nd insulator layers became independent, With said 1st and 2nd control electrodes, it becomes independent, and it has further the 1st main electrode formed in contact with said 1st and 2nd semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer, and is constituted.
[0012] Moreover, the 1st semi-conductor layer of the 1st conductivity type with which the semiconductor device concerning the 3rd invention has the 1st principal plane and the 2nd principal plane, The 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of

said 1st semi-conductor layer, The 1st semiconductor region of the 2nd conductivity type alternatively formed on said 2nd principal plane of said 1st semi-conductor layer, The 2nd semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which was alternatively formed in front face of said 1st semiconductor region / semi-conductor ], The 1st insulator layer of said 1st semiconductor region and said 2nd semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in the other side side of said 1st and 2nd semiconductor regions which counter said one side side, The 3rd semiconductor region of the 2nd control electrode formed on said 2nd insulator layer, and the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 1st insulator layer, The 4th semiconductor region of the 2nd conductivity type alternatively formed in the front face of said 1st semiconductor region in contact with said 2nd insulator layer, With said 1st and 2nd control electrodes, it becomes independent, and it has the 1st main electrode formed in contact with said 2nd, 3rd, and 4th semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer, and is constituted.

[0013] Moreover, the 1st semi-conductor layer of the 1st conductivity type with which the semiconductor device concerning the 4th invention has the 1st principal plane and the 2nd principal plane, The 2nd semi-conductor layer of the 2nd conductivity type formed on said 1st principal plane of said 1st semi-conductor layer, The 1st semiconductor region of the 2nd conductivity type alternatively formed on said 2nd principal plane of said 1st semi-conductor layer, The 2nd semiconductor region of the 1st conductivity type of low resistance [ layer / said / 1st / which was alternatively formed in said 1st semiconductor region front face / semi-conductor ], The 1st insulator layer of said 1st semiconductor region and said 2nd semiconductor region formed in the side face on the other hand, The 1st control electrode formed on said 1st insulator layer, and the 2nd insulator layer formed in the other side side of said 1st and 2nd semiconductor regions which counter said one side side, So that the 2nd control electrode formed on said 2nd insulator layer may be touched at said 1st and 2nd insulator layers both The 3rd semiconductor region of the 2nd conductivity type which consists of a discrete field where the plurality which was alternatively formed in said 1st semiconductor region front face, and was located in a line along with these 1st and 2nd insulator layers became independent, With said 1st and 2nd control electrodes, it becomes independent, and it has the 1st main electrode formed in contact with said 2nd and 3rd semiconductor regions, and the 2nd main electrode formed in contact with said 2nd semi-conductor layer, and is constituted.

[0014] Moreover, the manufacture approach of the semiconductor device concerning the 5th invention (a) The process which forms the 2nd semi-conductor layer of the 2nd conductivity type on said 1st principal plane of the 1st semi-conductor layer of the 1st conductivity type which has the 1st principal plane and the 2nd principal plane, (b) The process which forms heights alternatively on said 2nd principal plane of said 1st semi-conductor layer, (c) -- the top face of said heights of said 1st semi-conductor layer -- this -- with the process which forms alternatively the 1st semiconductor region of the 1st conductivity type of low resistance from the 1st semi-conductor layer (d) Said heights of said 1st semi-conductor layer, and the process of said 1st semiconductor region which forms the 1st insulator layer in a side face on the other hand, (e) The process which forms the 1st control electrode on said 1st insulator layer, and the process which forms the 2nd insulator layer in said heights which counter the (f) aforementioned one side side, and the other side side of said 1st semiconductor region, (g) The process which forms the 2nd control electrode on said 2nd insulator layer, and the process which forms the 2nd semiconductor region of the 2nd conductivity type in the front face of the 1st semiconductor region of (h) above alternatively in contact with said 1st insulator layer, (i) The process which forms the 3rd semiconductor region of the 2nd conductivity type in the front face of said 1st semiconductor region alternatively in contact with said 2nd insulator layer, (j) With said 1st and 2nd control electrodes, it becomes independent, and it has the process which forms the 1st main electrode which touched said 1st, 2nd, and 3rd semiconductor regions, and the process which forms the 2nd main electrode which touched the semi-conductor layer of the (k) above 2nd, and is constituted.

[0015] Moreover, the manufacture approach of the semiconductor device concerning the 6th invention

said process (c), and said said process (h) and said process (i) -- said 2nd principal plane of said 1st semi-conductor layer -- alternative -- the impurity of the 1st conductivity type -- being spread -- this -- with the process which forms said 1st semiconductor region of low resistance from the 1st semi-conductor layer [ a process (b), and ] The process which diffuses the impurity of the 2nd conductivity type alternatively on the front face of this 1st semiconductor region, and forms said 2nd and 3rd semiconductor regions in coincidence, It has the process which forms the slot on the pair so that the 2nd principal plane of the 1st semi-conductor layer may become convex. a part of said 1st, 2nd, and 3rd semiconductor region and said 1st semi-conductor layer -- alternative -- coincidence -- etching -- these 1st, 2nd, and 3rd semiconductor regions -- this -- It has the process at which said process (d) and said process (f) form said 1st and 2nd insulator layers in coincidence by forming an insulator layer in the front face of the slot of said pair. By forming a conductor in Mizouchi of said pair in which said insulator layer was formed, said process (e) and said process (g) are equipped with the process which forms said 1st and 2nd control electrodes in coincidence, and are constituted.

[0016]

[Function] When the 2nd semiconductor region of the 2nd conductivity type and the 3rd semiconductor region of the 2nd conductivity type in the 1st invention carry out the turn-off of the semiconductor device by carrying out bias of the 1st and 2nd control electrodes suitably to the 1st main electrode, the role which draws out the carrier poured in through the inversion layer formed in the 1st semiconductor region which meets the 1st and 2nd control electrodes is played. Therefore, resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 1st whole semiconductor region is used for a turn-on and a turn-off and the area effectiveness of the 1st semiconductor region in which conductivity modulation is made to start is [ there is little commutation of a carrier and ] good, the rise of ON state voltage can be prevented.

[0017] Moreover, the 2nd semiconductor region of the 2nd conductivity type in the 2nd invention plays the role which draws out the carrier poured in through the inversion layer formed in the 1st semiconductor region which meets the 1st and 2nd control electrodes, when carrying out the turn-off of the semiconductor device by carrying out bias of the 1st and 2nd control electrodes suitably to the 1st main electrode. Therefore, resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 1st whole semiconductor region is used for a turn-on and a turn-off and the area effectiveness of the 1st semiconductor region in which conductivity modulation is made to start is [ there is little commutation of a carrier and ] good, the rise of ON state voltage can be prevented.

[0018] Moreover, when the 3rd semiconductor region of the 2nd conductivity type and the 4th semiconductor region of the 2nd conductivity type in the 3rd invention carry out the turn-off of the semiconductor device by carrying out bias of the 1st and 2nd control electrodes suitably to the 1st main electrode, the role which draws out the carrier poured in through the inversion layer formed in the 2nd semiconductor region which meets the 1st and 2nd control electrodes is played. Therefore, resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 2nd whole semiconductor region is used for a turn-on and a turn-off and the area effectiveness of the 2nd semiconductor region in which conductivity modulation is made to start is [ there is little commutation of a carrier and ] good, the rise of ON state voltage can be prevented.

[0019] Furthermore, since direct pressure-proofing is held between the 1st semiconductor region of the 2nd conductivity type, and the 1st semi-conductor layer of the 1st conductivity type, a semiconductor device can be made thin. Moreover, a semiconductor device can also be made into an OFF state by adjusting the high impurity concentration of the 1st semiconductor region, for example in the condition of not carrying out bias of the 1st and 2nd control electrodes.

[0020] Moreover, the 3rd semiconductor region of the 2nd conductivity type in the 4th invention plays the role which draws out the carrier poured in through the inversion layer formed in the 2nd semiconductor region which meets the 1st and 2nd control electrodes, when carrying out the turn-off of

the semiconductor device by carrying out bias of the 1st and 2nd control electrodes suitably to the 1st main electrode. Therefore, resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 2nd whole semiconductor region is used for a turn-on and a turn-off and the area effectiveness of the 2nd semiconductor region in which conductivity modulation is made to start is [ there is little commutation of a carrier and ] good, the rise of ON state voltage can be prevented.
[0021] Furthermore, since direct pressure-proofing is held between the 1st semiconductor region of the 2nd conductivity type, and the 1st semi-conductor layer of the 1st conductivity type, a semiconductor device can be made thin. Moreover, a semiconductor device can also be made into an OFF state by adjusting the high impurity concentration of the 1st semiconductor region, for example in the condition of not carrying out bias of the 1st and 2nd control electrodes.
[0022] Moreover, the process which forms the 2nd semiconductor region of the 2nd conductivity type in the front face of said 1st semiconductor region in the manufacture approach of the semiconductor device the 5th invention alternatively in contact with said 1st insulator layer, With the process which forms the 3rd semiconductor region of the 2nd conductivity type in the front face of said 1st semiconductor region alternatively in contact with said 2nd insulator layer Since the 2nd and 3rd semiconductor regions are formed in the front face of the 1st semiconductor region, the 2nd and 3rd semiconductor regions can be easily formed with ion-implantation etc.
[0023] Moreover, since the process which diffuses the impurity of the 2nd conductivity type alternatively on the front face of the 1st semiconductor region in the manufacture approach of the semiconductor device the 6th invention, and forms said 2nd and 3rd semiconductor regions in coincidence forms the semiconductor region of the 2nd conductivity type in the front face of the 1st semiconductor region by diffusion of an impurity, it can form the 2nd and 3rd semiconductor regions that it is simultaneous and easily.
[0024]
[Example] Hereafter, the 1st example of this invention is explained using drawing 1 thru/or drawing 5 . Drawing 1 and drawing 2 are the top views and sectional views showing the structure of the semiconductor device by the 1st example of this invention. Setting to drawing, 1 is n. - An epitaxial layer and 2 are p+. A substrate and 3 are n. - Heights formed in the front face of an epitaxial layer 1, 4 is n+ formed in the top face of heights 3. A diffusion field and 5 are n. - The inferior surface of tongue of the heights 3 of an epitaxial layer 1, a side face on either side, and n+ The insulator layer formed in the side face of right and left of the diffusion field 4, For two gate electrodes which 6 has in right and left of heights 3, and 8, an insulator layer and 7 are n+. p+ prepared in the trailer of the diffusion field 4 Diffusion field, 13 is n+. p+ formed so that the front face of the diffusion field 4 might be touched at an insulator layer 5 A diffusion field and 9 are n+. The diffusion field 4 and p+ The aluminum-Si electrode formed so that the diffusion field 13 might be contacted, and 10 are p+. It is a metal electrode in contact substrate 2. In addition, in drawing 1 , in order to make structure of this invention intelligible, an electrode 9 and the top view except an insulator layer 8 are shown, and the electrode from which the Y-Y sectional view of drawing 1 was excluded by drawing 1 is indicated and shown in drawing 2 at it.
[0025] Next, actuation of this semiconductor device is explained using drawing 3 thru/or drawing 5 . n which is between control electrodes 6 when the potential of the control electrode 6 to an electrode 9 is lowered in drawing 3 , where the potential of the electrode 10 to an electrode 9 is raised - When the depletion layer extended from a control electrode 6 touches the heights 3 of an epitaxial layer 1 mutually, a potential barrier arises. Therefore, an electron will not flow toward an electrode 10 from an electrode 9. Thus, it can change into a current inhibition condition.
[0026] Next, if the potential of the control electrode 6 to an electrode 9 is raised, said potential barrier will disappear and an electron 12 will begin to flow toward an electrode 10 from an electrode 9. It is p+ to this and coincidence. A hole 11 is poured in from a substrate 2 and it is n. - Conductivity modulation is started by the epitaxial layer 1. The hole 11 poured in as shown in drawing 4 is n. - An epitaxial layer 1 or n+ Since it re-joins in the diffusion field 4, conductivity modulation can fully be started. Thus, the turn-on of the semiconductor device can be carried out. This time n+ n of the diffusion field 4 - All the

fields that touch an epitaxial layer 1 are used, and there is no rise of ON state voltage compared with the former.
[0027] Next, if the potential of the control electrode 6 to an electrode 9 is lowered again, a potential barrier will arise again in the heights 3 between control electrodes 6, and the electron current will not flow toward an electrode 10 from an electrode 9. And it is n+ which it is transmitted to a front face as the hole 11 poured into coincidence at this time is accumulated in the front face of an insulator layer 5 as shown in drawing 5 , and meets an electrode 6. It passes along p inversion layer formed in the side face of the diffusion field 4, and is p+. It is drawn out from the diffusion field 13 to an electrode 9. Thus, the turn-off of the semiconductor device can be carried out. Therefore, resistance in case a hole 11 is drawn out is small, since the distance which the hole 11 drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick.
[0028] With the semiconductor device which has such structure, it is n+. It is p+, even if it enlarges the diffusion field 4 and lowers ON state voltage. If the diffusion field 13 is formed suitably, the resistance when drawing out a hole 11 and distance are seldom influenced, but a switching loss will be small and will become possible [ that switching speed also forms a semiconductor device with low ON state voltage quickly ]. In addition, in drawing, the dotted line shows the equipotential line. Moreover, p+ conventionally used for the drawing of a hole 11 The diffusion field 7 contributes to relaxation of the electric-field concentration for a trailer, and most duties of the drawing of a hole 11 are not ******(ing) it.
[0029] Next, the 2nd example of this invention is explained using drawing 6 thru/or drawing 8 . Drawing 6 is the sectional view of the semiconductor device by the 2nd example. Setting to drawing, 14 is n. - p+ of an epitaxial layer 1 formed in the principal plane on the other hand It is a diffusion field and is in contact with the metal electrode 10. Moreover, a metal electrode 10 is n. - It is in contact also with the epitaxial layer 1. And the part of the same sign as other 1st example shows the same as that of the 1st example, or a considerable part.
[0030] First, the actuation in a current inhibition condition is the same as that of the semiconductor device of the 1st example. And if the potential of the control electrode 6 to an electrode 9 is raised from the current inhibition condition, a potential barrier will disappear and an electron will begin to flow toward an electrode 10. It is p+ by the voltage drop by this electron current. The diffusion field 14 and n - Forward bias is added between epitaxial layers 1, and it is p+. A hole 11 is poured in from the diffusion field 14, and it is n. - Conductivity modulation is started by the epitaxial layer 1. Most holes 11 poured in as shown in drawing 7 are n altogether. - An epitaxial layer 1 or n+ Since it recombines in the diffusion field 4, conductivity modulation can fully be started. Thus, the turn-on of the semiconductor device can be carried out.
[0031] Next, if the potential of the control electrode 6 to an electrode 9 is lowered again, a potential barrier will arise again in the heights 3 between electrodes 6, and the electron current will not flow toward an electrode 10 from an electrode 9. The hole 11 poured into coincidence as shown in drawing 8 is n+ which is transmitted to a front face as is accumulated in the front face of an insulator layer 5, and meets a control electrode 6. It passes along p inversion layer formed in the side face of the diffusion field 4, and is p+. It is drawn out from the diffusion field 13 to an electrode 9. Thus, a turn-off can be carried out.
[0032] Moreover, it sets at the time of a turn-off, and is p+. Stopping, when the impregnation from the diffusion field 14 is quick, and n - The electron current in an epitaxial layer 1 is an electrode 10 and n. - By mainly flowing the part with which the epitaxial layer 1 is in contact, turn-off speed can be made quick and a turn-off loss can be lessened.
[0033] Next, the 3rd example of this invention is explained using drawing 9 . Drawing 9 is the sectional view of the semiconductor device by the 3rd example of this invention. drawing -- setting -- 15 -- p+ n+ formed in the front face of a substrate 2 a field and 16 -- p+ n+ formed on the substrate It is a semi-conductor layer. And a metal electrode 10 is p+. A substrate 2 and n+ It is in contact with both fields 15. In addition, the same sign as other 1st example being the same as that of the 1st example or a considerable part is shown.

[0034] Where the potential of the electrode 10 to the electrode 9 of the semiconductor device shown in drawing 9 is raised, when the potential of the control electrode 6 to an electrode 9 is lowered, it is n between electrodes 5. - Since a potential barrier arises to electronic energy in the heights 3 of an epitaxial layer 1 by depletion-ization, an electron will not flow toward an electrode 10 from an electrode 9. A depletion layer is n+. It is n+ when the semi-conductor layer 16 is reached. For the semi-conductor layer 16, a depletion layer is p+. It has the function which prevents reaching a substrate 1. And it is n+ to other examples. The same effectiveness is done so even if it uses the semi-conductor layer 16. Thus, it can change into a current inhibition condition.
[0035] Next, if the potential of the control electrode 6 to an electrode 9 is raised, said potential barrier will disappear and an electron will begin to flow toward an electrode 10 from an electrode 9. It can come, simultaneously is p+. A hole 11 is poured in from a substrate 2 and it is n. - Conductivity modulation is started by the epitaxial layer 1. Most poured-in holes 11 are n altogether. - An epitaxial layer 1 or n+ Since it recombines in a semiconductor region 4, conductivity modulation can fully be started. Thus, the turn-on of the semiconductor device can be carried out.
[0036] Here, it is n+. The semi-conductor layer 16 has the work which suppresses impregnation of a hole 11, generally is the structure of this part and is optimizing the injection rate of a hole 11. On the other hand, it is n+. A field 15 has the work which suppresses impregnation of a hole 11 in high current density. Therefore, the n+ field 15 and n+ By combining the semi-conductor layer 16, below by the rated current, a current tends to flow and the property which beyond the rated current cannot flow easily and a semiconductor device cannot destroy easily is acquired.
[0037] Next, when the potential of the control electrode 6 to an electrode 9 is lowered again, it is n between control electrodes 6. - A potential barrier will arise in the heights 3 of an epitaxial layer 1, and the electron current will not flow toward an electrode 10 from an electrode 9. The hole 11 poured into coincidence is n+ which is transmitted to a front face as is accumulated in the front face of an insulator layer 5, and meets a control electrode 6. It passes along p inversion layer formed in the side face of the diffusion field 4, and is p+. It is drawn out from the diffusion field 13 to an electrode 9. Thus, the turn-off of the semiconductor device can be carried out.
[0038] Next, the 4th example of this invention is explained using drawing 10 . Drawing 10 is the sectional view of the semiconductor device by the 4th example of this invention. Setting to drawing, 17 is an insulator layer 6 and n. - It is p diffusion field formed between epitaxial layers 1. In addition, the same sign as other 1st example being the same as that of the 1st example or a considerable part is shown.
[0039] Where the potential of the electrode 10 to the electrode 9 of the semiconductor device shown in drawing 10 is raised, when the potential of the control electrode 6 to an electrode 9 is lowered, it is n between electrodes 5. - Since a potential barrier arises to electronic energy in the heights 3 of an epitaxial layer 1 by depletion-ization, an electron will not flow toward an electrode 10 from an electrode 9. Thus, it can change into a current inhibition condition. At this time, p diffusion field 17 is an insulator layer 5 and n. - Since the electric field between epitaxial layers 1 are eased, it becomes easier to come out of pressure-proofing when a semiconductor device carries out a turn-off. This situation is shown in drawing 11 . It is drawing showing distribution of the electric field in alignment with B-B' in case the p diffusion layer 17 has drawing and drawing 11 (d) which show distribution of the electric field in alignment with A-A' in case the p diffusion layer 17 does not have the equipotential line of control-electrode 6 near in case the p diffusion layer 17 has the equipotential line of control-electrode 6 near in case the p diffusion layer 17 does not have drawing 11 (a), and drawing 11 (b), and drawing 11 (c). This drawing is a schematic diagram for helping an understanding. And pressure-proofing can be secured even if it makes the depth of a control electrode 6 shallow, as shown in this drawing.
[0040] Next, if the potential of the control electrode 6 to an electrode 9 is raised, said potential barrier will disappear and an electron will begin to flow toward an electrode 10 from an electrode 9. It can come, simultaneously is p+. When shown in drawing 4 from a substrate 2, a hole 11 is poured in similarly, and it is n. - Conductivity modulation is started by the epitaxial layer 1. Most poured-in holes 11 are the n-epitaxial layer 1 or n+ altogether. Since it recombines in a semiconductor region 4,

conductivity modulation can fully be started. Thus, the turn-on of the semiconductor device can be carried out.
[0041] Next, when the potential of the control electrode 6 to an electrode 9 is lowered again, it is n between control electrodes 6. - In the heights 3 of an epitaxial layer 1, a potential barrier will arise again, and the electron current will not flow from an electrode 9 toward an electrode 10 to them. It is n+ which the hole 11 similarly poured into coincidence will flow into p diffusion field 17 of the front face of an insulator layer 5, and will meet a control electrode 6 if shown in drawing 5 . It passes along p inversion layer formed in the side face of the diffusion field 4, and is p+. It is drawn out from the diffusion field 13 to an electrode 9. Thus, the turn-off of the semiconductor device can be carried out. There is effectiveness which makes turn-off speed quick since p diffusion field 17 lowers the resistance in the drawing of a hole 11 here, and lessens a turn-off loss.
[0042] Next, the 5th example of this invention is explained using drawing 12 . Drawing 12 is the sectional view of the semiconductor device by the 5th example of this invention. drawing -- setting -- 18 -- n+ The diffusion field 4 and n- p- formed between the top faces of the heights 3 of an epitaxial layer 1 It is a field. In addition, the same sign as the 1st example being the same as that of the 1st example or a considerable part is shown.
[0043] Where the potential of the electrode 10 to the electrode 9 of the semiconductor device shown in drawing 12 is raised, when the potential of the control electrode 6 to an electrode 9 is lowered, it is n between electrodes 5. - Since a potential barrier arises to electronic energy in the heights 3 of an epitaxial layer 1 by depletion-ization, an electron will not flow toward an electrode 10 from an electrode 9. Thus, it can change into a current inhibition condition. At this time p - For a field 18, a depletion layer is n+. Since there is effectiveness which prevents arriving at the diffusion field 4, it becomes unnecessary to lower the electrical potential difference of a control electrode 6 not much, and no MARIOFU is also possible. p- It is p when the high impurity concentration of a field 18 is raised. - A field 18 and n - It becomes possible to be able to hold direct pressure-proofing between epitaxial layers 1, i.e., to change into a current inhibition condition, without building a potential barrier. And n - The example which lost the heights 3 formed in the front face of an epitaxial layer 1 is shown in drawing 13 . Thus, a semiconductor device can be constituted thinly.
[0044] Next, if the potential of the control electrode 6 to an electrode 9 is raised, said potential barrier will disappear and an electron will begin to flow toward an electrode 10 from an electrode 9. At this time, it is p. - It is n+ when a field 18 depletion-izes completely. The diffusion field 4 and p - Impregnation of an electron arises from the whole junction of a field 18. On the other hand, it is p. - It is p even when the field 18 has not depletion-ized completely. - The electron current is able for the part which met the control electrode 6 of a field 18 to carry out n reversal, to carry out, and to drop off through this n inversion layer. It can come, simultaneously is p+. A hole 11 is poured in from a substrate 2 and it is n. - Conductivity modulation is started by the epitaxial layer 1. Most poured-in holes 11 are n altogether. - An epitaxial layer 1, p - A field 18 or n+ Since it recombines in a semiconductor region 4, conductivity modulation can fully be started. Since it has thyristor structure of npnp in the case of this structure, it is also considered that a latch property is shown. Thus, the turn-on of the semiconductor device can be carried out.
[0045] Next, when the potential of the control electrode 6 to an electrode 9 is lowered again, it is n between control electrodes 6. - A potential barrier will arise again in the heights 3 of an epitaxial layer 1, and the electron current will not flow toward an electrode 10 from an electrode 9. The hole 11 poured into coincidence is n+ which is transmitted to a front face as is accumulated in the front face of an insulator layer 5, and meets a control electrode 6. It passes along p inversion layer formed in the side face of the diffusion field 4, and is p+. It is drawn out from the diffusion field 13 to an electrode 9. Thus, the turn-off of the semiconductor device can be carried out.
[0046] In addition, at the above 1st to the 5th example, it is p+. The diffusion field 13 is n. - It is p+ as it is shown in drawing 14 in the case of structure like the 1st example for example, although the case of not being in contact with an epitaxial layer 1 was shown. The diffusion field 13 is n. - It may be in contact with the epitaxial layer 1, and the same effectiveness as each above-mentioned example is done

so. However, the drawing of the hole 11 at the time of carrying out a turn-off in this case is n+. Not only passing along p inversion layer formed in the diffusion field 4 but direct p+ It is drawn out through the diffusion field 13. Moreover, at the 4th and 5th examples, it is p+. The diffusion field 13 is p diffusion field 17 and p directly. - It is required to make it not touch a field 18.

[0047] Next, the 6th example is explained using drawing 15 thru/or drawing 16 . Drawing 15 and drawing 16 are the top views and sectional views showing the structure of the semiconductor device by the 6th example of this invention. Setting to drawing, 1 is n. - An epitaxial layer and 2 are p+. A substrate and 3 are n. - Heights formed in the front face of an epitaxial layer 1, 4 is n+ formed in the top face of heights 3. A diffusion field and 5 are n. - The inferior surface of tongue of the heights 3 of an epitaxial layer 1, a side face on either side, and n+ The insulator layer formed in the side face of right and left of the diffusion field 4, For two gate electrodes which 6 has in right and left of heights 3, and 8, an insulator layer and 7 are n+. p+ prepared in the trailer of the diffusion field 4 A diffusion field and 20 are n+. Two or more p+ formed so that the insulator layer 5 of right and left on the front face of the diffusion field 4 might be touched It is a diffusion field. This p+ The diffusion field 20 is n+ as shown in drawing. It is discretely formed in the diffusion field 4 independently, respectively. And 9 is n+. The aluminum-Si electrode formed so that the diffusion field 4 and p+ diffusion field 20 might be contacted, and 10 are p+. It is a metal electrode in contact substrate 2. In addition, in drawing 15 , in order to make structure of this invention intelligible, an electrode 9 and the top view except an insulator layer 8 are shown, and a part of electrode which excluded the insulator layer 5 in some control electrodes 6 currently drawn by drawing 15 in the Z-Z sectional view of drawing 15 , and was excluded by drawing 15 is indicated and shown in drawing 16 at it.

[0048] Thus, the semiconductor device of the 1st example is n. - p+ diffusion fields formed in the diffusion field 4 differ. Namely, p+ formed in the 1st example along with the insulator layer 5 currently formed in right and left of the heights 3 of a sectional view ( drawing 2 ) p which is the diffusion field 13 and was formed in the 6th example in contact with both the insulator layers 5 currently formed in right and left of the heights 3 of a sectional view ( drawing 2 ) - It is the diffusion field 20. However, although it is fundamentally [ about actuation and effectiveness / as the 1st example ] the same, at the 1st example, the width of face of heights 3 is an electrode 9 and p+. Although restricted by the allowances of contact to the diffusion field 13, since it is not necessary to see the allowances of contact in the 6th example, it becomes possible to form heights 3 more finely. By this, formation of the potential barrier at the time of a turn-off can become easy, can make turn-off speed still quicker, and can lessen a turn-off loss further.

[0049] Therefore, the combination of the 2nd example to the 6th example and the 5th example is also possible, and actuation and effectiveness are the same as each example. First, the sectional view at the time of combining the 6th example and the 2nd example is shown in drawing 17 . Next, the sectional view at the time of combining the 6th example and the 3rd example is shown in drawing 18 . Next, the sectional view at the time of combining the 6th example and the 4th example is shown in drawing 19 . Next, the sectional view at the time of combining the 6th example and the 5th example is shown in drawing 20 and drawing 21 .

[0050] Moreover, it is p+ also about the 6th example. The diffusion field 20 is n. - It is p+ as it is shown in drawing 22 in the case of structure like the 1st example for example, although the case of not being in contact with an epitaxial layer 1 was shown. The diffusion field 20 is n. - It may be in contact with the epitaxial layer 1, and the same effectiveness as each above-mentioned example is done so. However, the drawing of the hole 11 at the time of carrying out a turn-off in this case is n+. Not only passing along p inversion layer formed in the diffusion field 4 but direct p+ It is also possible to draw out through the diffusion field 20. Moreover, although the same is said of combination with the 2nd to 5th example, at the 4th and 5th examples, it is p+. The diffusion field 20 is p diffusion field 17 and p directly. - It is required to make it not touch a field 18.

[0051] Next, the manufacture approach of the semiconductor device shown in drawing 1 and drawing 2 is explained using drawing 23 thru/or drawing 29 . First, p+ The n-epitaxial layer 32 is formed with an epitaxial grown method on a substrate 31.

[0052] Next, it is n as shown in drawing 23 . - After forming a resist on an epitaxial layer 31, the impurity of n mold is poured in by using a resist as a mask, annealing is performed after resist removal, and it is n+. The diffusion field 33 is formed.
[0053] Next, it is n+ as shown in drawing 24 . The underlay oxide film 34 is formed the whole surface on the diffusion field 33, and a resist 35 is formed on the underlay oxide film 34. Then, patterning of the resist 35 is carried out and the aperture for impurity impregnation is opened.
[0054] Next, the impurity of p mold is poured in from the aperture opened in the resist 35 as shown in drawing 25 , annealing is performed, and it is p+. The diffusion field 36 is formed.
[0055] Next, as shown in drawing 26 , the underlay oxide film 34 and a resist 35 are removed, and the underlay oxide film 37 and a nitride 38 are formed anew. Then, patterning of the underlay oxide film 37 and a nitride 38 is performed.
[0056] Next, it is n, using as a mask the underlay oxide film 37 and nitride 38 by which patterning was carried out as shown in drawing 27 . - It etches deeply to the middle of an epitaxial layer 32, and a slot 41 is formed alternatively. The anisotropic etching of others [ dry etching ] is sufficient as this etching.
[0057] Next, as shown in drawing 28 , after forming an oxide film 39 in the inside of a slot 41 thinly, polish recon is deposited all over including the interior of a slot 41, and the gate electrode 40 is formed by performing etchback and leaving polish recon only to the interior of a slot 41. Then, an oxide film 42 is formed in the whole surface by the oxidizing [ thermally ] method.
[0058] Next, as shown in drawing 29 , using the thinness of the thickness of the oxide film 42 on a nitride 38, oxide film etching is performed, only a nitride 38 is exposed, further, nitride etching is performed and a nitride 38 is removed. And patterning of the underlay oxide film 37 is carried out, sputter deposition of the ARUMI silicon is carried out to the whole surface, and an electrode 43 is formed in it. Then, an electrode 44 is formed further.
[0059] In addition, it is n as it is shown in drawing 35 , after forming the slot 41 shown in drawing 27 . - The p diffusion layer 45 is formed in the front face of an epitaxial layer 32 by diffusing p mold impurity. Thus, p diffusion field 17 shown in drawing 10 can be formed easily, and the semiconductor device by said example and the 4th example shown in drawing 10 through the same process can be formed easily after that. At this time, it is n+. All over the diffusion field 33, since the concentration of n mold impurity is high, the field of p mold is not formed.
[0060]
[Effect of the Invention] As mentioned above, according to invention according to claim 1, a semiconductor device is equipped with the 2nd semiconductor region of the 2nd conductivity type, and the 3rd semiconductor region of the 2nd conductivity type, and is constituted. Said the 2nd semiconductor region and 3rd semiconductor region Since the role which draws out the carrier poured in through the inversion layer formed in the 1st semiconductor region is played when carrying out the turn-off of the semiconductor device Resistance in case a carrier is drawn out is small, and ** and a switching loss are [ the distance which the carrier drawn out moves is short and ] small, and switching speed also becomes quick. And since the 1st whole semiconductor region is used for a turn-on and a turn-off, the rise of ON state voltage can be prevented. Therefore, it is effective in successive diminution of the switching loss which suited the relation of a trade-off conventionally, and improvement in the speed of switching speed and the fall of ON state voltage being realizable for coincidence.
[0061] According to invention according to claim 2, a semiconductor device is equipped with the 2nd semiconductor region of the 2nd conductivity type, and is constituted. Moreover, said 2nd semiconductor region Since the role which draws out the carrier poured in through the inversion layer formed in the 1st semiconductor region is played when carrying out the turn-off of the semiconductor device Resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 1st whole semiconductor region is used for a turn-on and a turn-off, the rise of ON state voltage can be prevented. Therefore, it is effective in successive diminution of the switching loss which suited the relation of a trade-off conventionally, and improvement in the speed of switching speed and the fall of ON state voltage being realizable for coincidence. Furthermore, it is effective in the ability to form

heights more thinly, make turn-off speed still quicker, and lessen a turn-off loss further.
[0062] According to invention according to claim 3, a semiconductor device is equipped with the 3rd semiconductor region of the 2nd conductivity type, and the 4th semiconductor region of the 2nd conductivity type, and is constituted. Moreover, said 3rd and 4th semiconductor regions Since the role which draws out the carrier poured in through the inversion layer formed in the 2nd semiconductor region is played when carrying out the turn-off of the semiconductor device Resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 2nd whole semiconductor region is used for a turn-on and a turn-off, the rise of ON state voltage can be prevented. Therefore, it is effective in successive diminution of the switching loss which suited the relation of a trade-off conventionally, and improvement in the speed of switching speed and the fall of ON state voltage being realizable for coincidence.
[0063] Furthermore, the semiconductor device is equipped with the 1st semiconductor region of the 2nd conductivity type, and gets down, and it is effective in the ability to make a semiconductor device thin in order to hold direct pressure-proofing between the 1st semiconductor region of said 2nd conductivity type, and the 1st semi-conductor layer of the 1st conductivity type. Moreover, it is effective in the ability to make a semiconductor device into an OFF state in the condition of not carrying out bias of the 1st and 2nd control electrodes by adjusting the high impurity concentration of the 1st semiconductor region, for example.
[0064] According to invention according to claim 4, a semiconductor device is equipped with the 3rd semiconductor region of the 2nd conductivity type, and is constituted. Moreover, said 3rd semiconductor region Since the role which draws out the carrier poured in through the inversion layer formed in the 2nd semiconductor region is played when carrying out the turn-off of the semiconductor device Resistance in case a carrier is drawn out is small, since the distance which the carrier drawn out moves becomes short, a switching loss is small, and switching speed also becomes quick. And since the 2nd whole semiconductor region is used for a turn-on and a turn-off, the rise of ON state voltage can be prevented. Therefore, it is effective in successive diminution of the switching loss which suited the relation of a trade-off conventionally, and improvement in the speed of switching speed and the fall of ON state voltage being realizable for coincidence. Furthermore, it is effective in the ability to make turn-off speed still quicker and lessen [ can make thin spacing between the 1st and 2nd control electrodes, ] a turn-off loss further.
[0065] Furthermore, a semiconductor device is equipped with the 1st semiconductor region of the 2nd conductivity type, and is constituted, and it is effective in the ability to make a semiconductor device thin in order to hold direct pressure-proofing between the 1st semiconductor region of said 2nd conductivity type, and the 1st semi-conductor layer of the 1st conductivity type. Moreover, it is effective in the ability to make a semiconductor device into an OFF state in the condition of not carrying out bias of the 1st and 2nd control electrodes by adjusting the high impurity concentration of the 1st semiconductor region, for example.
[0066] Moreover, the process which forms the 2nd semiconductor region of the 2nd conductivity type in the front face of the 1st semiconductor region alternatively in contact with said 1st insulator layer according to the manufacture approach of a semiconductor device according to claim 5, Have the process which forms the 3rd semiconductor region of the 2nd conductivity type in the front face of the 1st semiconductor region alternatively in contact with said 2nd insulator layer, and it is constituted. The 2nd and 3rd semiconductor regions can be formed easily, and it is effective in the ability to manufacture the semiconductor device concerning this invention easily.
[0067] Moreover, according to the manufacture approach of a semiconductor device according to claim 6, it has the process which diffuses the impurity of the 2nd conductivity type alternatively on the front face of the 1st semiconductor region, and forms said 2nd and 3rd semiconductor regions in coincidence, and is constituted, the 2nd and 3rd semiconductor regions can be formed easily, and it is effective in the ability to manufacture the semiconductor device concerning this invention easily.

[Translation done.]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] It is the top view of the semiconductor device by the 1st example of this invention.
[Drawing 2] It is the Y-Y sectional view of the semiconductor device shown in drawing 1 .
[Drawing 3] It is the sectional view showing the current inhibition condition of the semiconductor device by the 1st example of this invention.
[Drawing 4] It is the sectional view showing the condition of the turn-on of the semiconductor device by the 1st example of this invention.
[Drawing 5] It is the sectional view showing the condition of the turn-off of the semiconductor device by the 1st example of this invention.
[Drawing 6] It is the sectional view of the semiconductor device by the 2nd example of this invention.
[Drawing 7] It is the sectional view showing the condition of the turn-on of the semiconductor device by the 2nd example of this invention.
[Drawing 8] It is the sectional view showing the condition of the turn-off of the semiconductor device by the 2nd example of this invention.
[Drawing 9] It is the sectional view of the semiconductor device by the 3rd example of this invention.
[Drawing 10] It is the sectional view of the semiconductor device by the 4th example of this invention.
[Drawing 11] It is drawing showing the situation of the electric field of the semiconductor device shown in drawing 10 and drawing 1 .
[Drawing 12] It is the sectional view of the semiconductor device by the 5th example of this invention.
[Drawing 13] It is the sectional view of other semiconductor devices by the 5th example of this invention.
[Drawing 14] It is the top view of other semiconductor devices by the 1st example of this invention.
[Drawing 15] It is the top view of the semiconductor device by the 6th example of this invention.
[Drawing 16] It is the Z-Z strabism sectional view of the semiconductor device shown in drawing 15 .
[Drawing 17] It is the sectional view of the semiconductor device by the combination of the 6th example of this invention, and the 2nd example.
[Drawing 18] It is the sectional view of the semiconductor device by the combination of the 6th example of this invention, and the 3rd example.
[Drawing 19] It is the sectional view of the semiconductor device by the combination of the 6th example of this invention, and the 4th example.
[Drawing 20] It is the sectional view of the semiconductor device by the combination of the 6th example of this invention, and the 5th example.
[Drawing 21] It is the sectional view of other semiconductor devices by the combination of the 6th example of this invention, and the 5th example.
[Drawing 22] It is the top view of other semiconductor devices by the 6th example of this invention.
[Drawing 23] It is the sectional view showing the production process of the semiconductor device of this invention.
[Drawing 24] It is the sectional view showing the production process of the semiconductor device of this

invention.
[Drawing 25] It is the sectional view showing the production process of the semiconductor device of this invention.
[Drawing 26] It is the sectional view showing the production process of the semiconductor device of this invention.
[Drawing 27] It is the sectional view showing the production process of the semiconductor device of this invention.
[Drawing 28] It is the sectional view showing the production process of the semiconductor device of this invention.
[Drawing 29] It is the sectional view showing the production process of the semiconductor device of this invention.
[Drawing 30] It is the top view of the conventional semiconductor device.
[Drawing 31] It is X-X strabismus sectional view of the semiconductor device shown in drawing 30 .
[Drawing 32] It is the strabism sectional view showing the current inhibition condition of the conventional semiconductor device.
[Drawing 33] It is the strabism sectional view showing the condition of the turn-on of the conventional semiconductor device.
[Drawing 34] It is the strabism sectional view showing the condition of the turn-off of the conventional semiconductor device.
[Drawing 35] It is the sectional view showing other production processes of the semiconductor device of this invention.
[Description of Notations]
1 N - Epitaxial Layer
2 P+ Substrate
3 Heights
4 N+ Diffusion Field
5 Insulator Layer
6 Gate Electrode
7 P+ Diffusion Field
8 Insulator Layer
9 Aluminum-Si Electrode
10 Metal Electrode
13 P+ Diffusion Field
14 P+ Diffusion Field
15 N+ Diffusion Field
16 N+ Layer
17 P Diffusion Field
18 P - Field

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[Translation done.]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DRAWINGS

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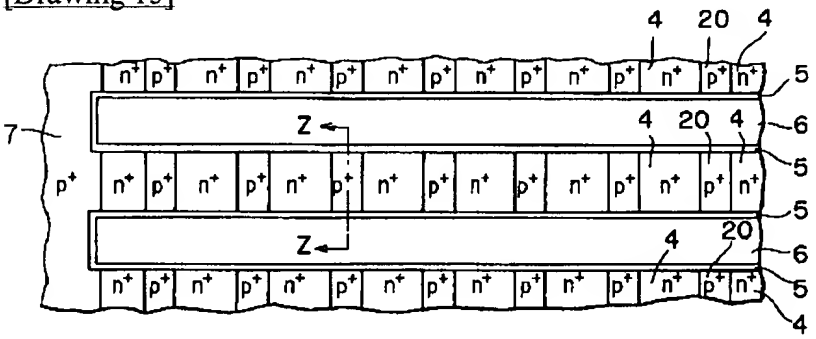
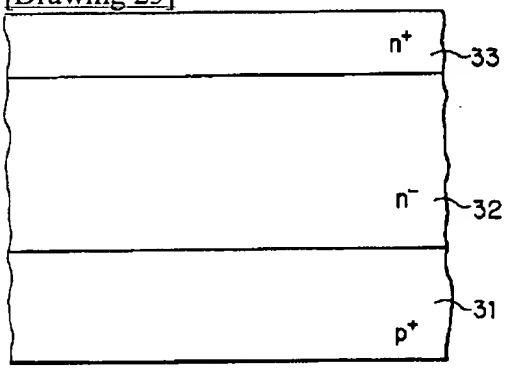
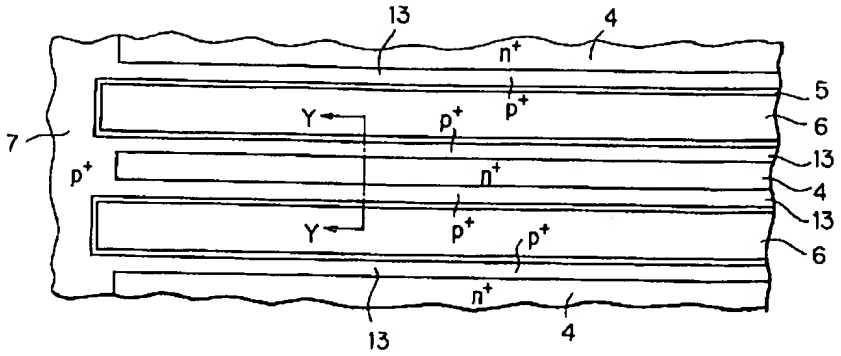
[Drawing 15]




[Drawing 23]

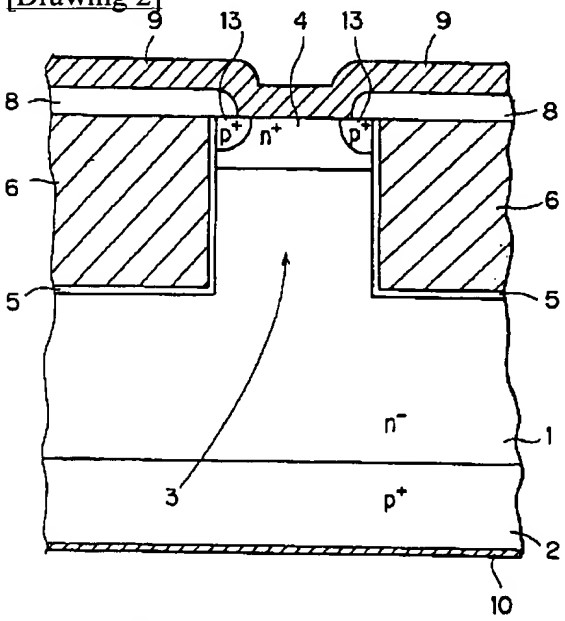



[Drawing 1]



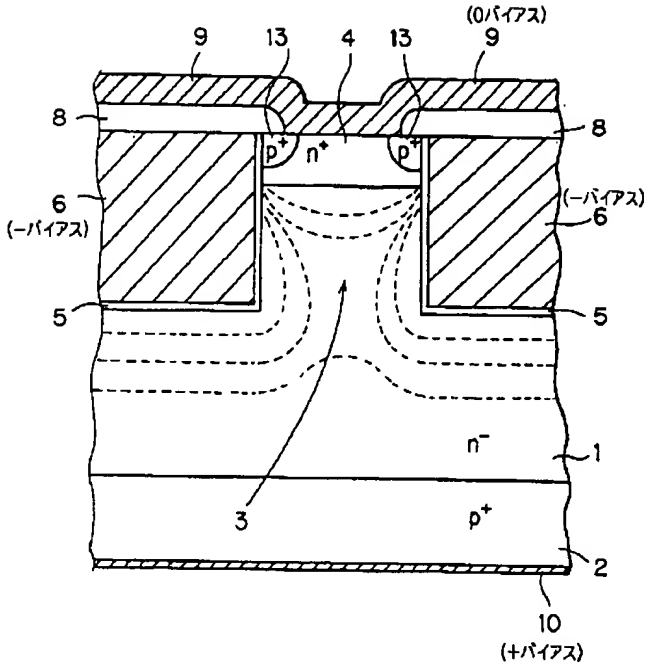

4:n+拡散領域
5:絶縁膜
6:ゲート電極
7:p+拡散領域
13:p+拡散領域

[Drawing 2]

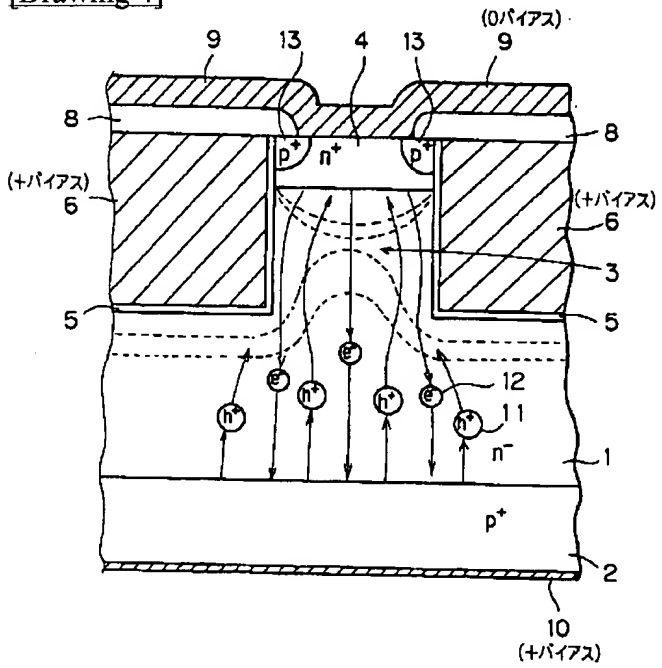



8:絶縁膜
9:Al−Si電極
10:金属電極

[Drawing 3]

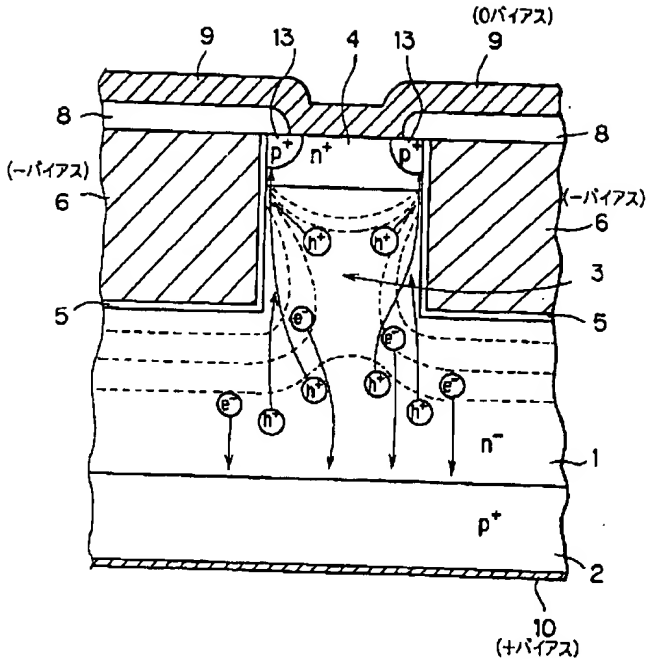



[Drawing 4]

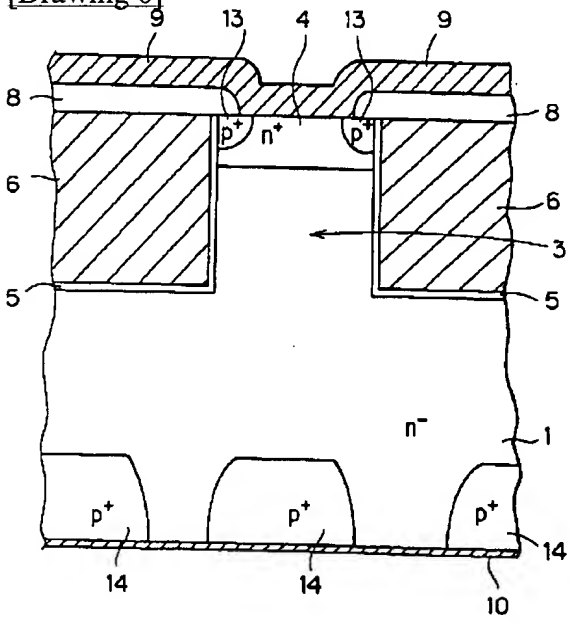



11:ホール
12:電子

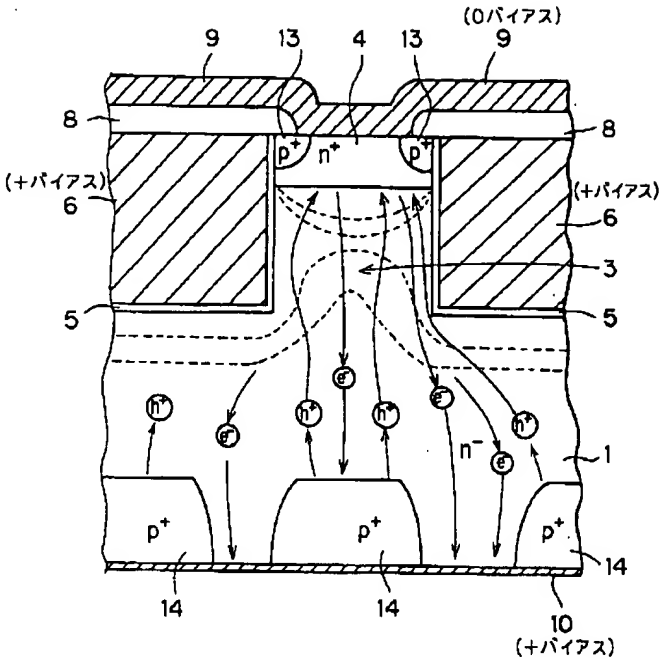
[Drawing 5]




[Drawing 6]




[Drawing 7]

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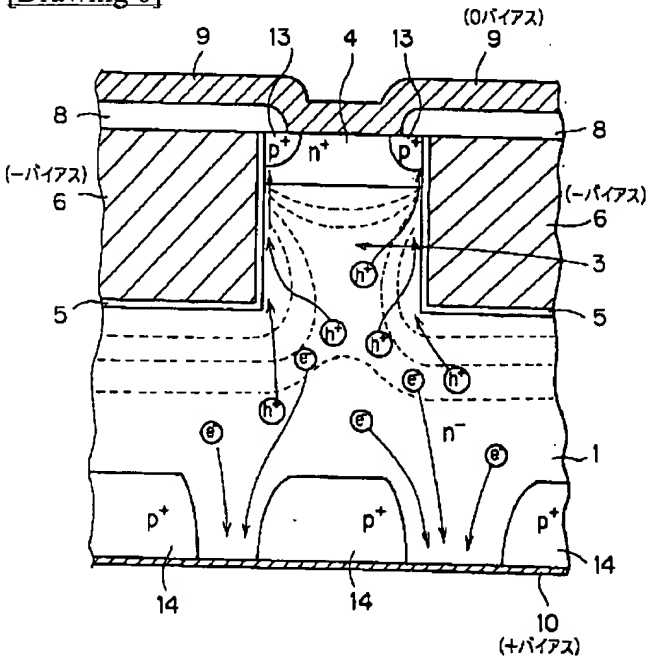
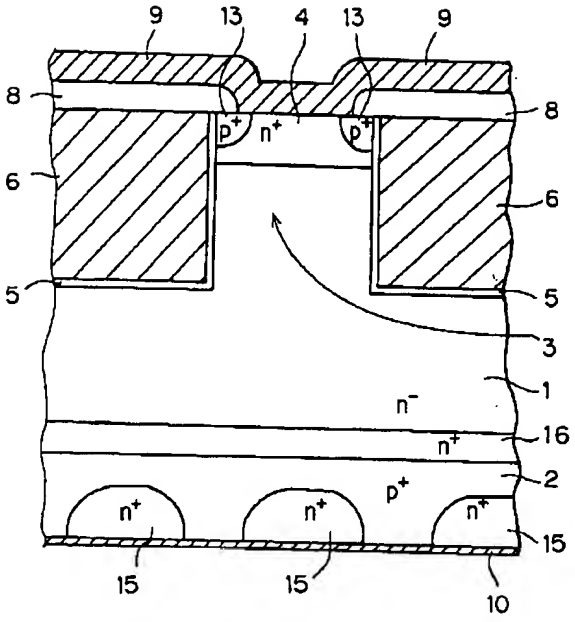



[Drawing 9]

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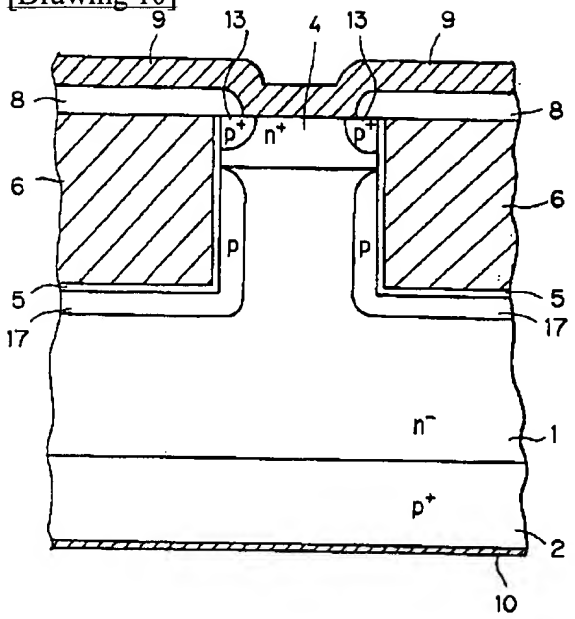


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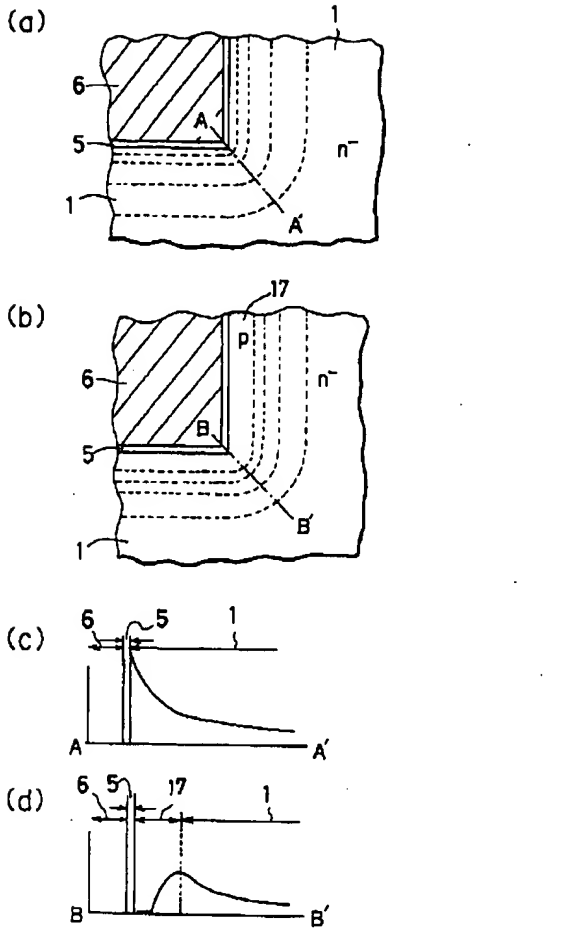


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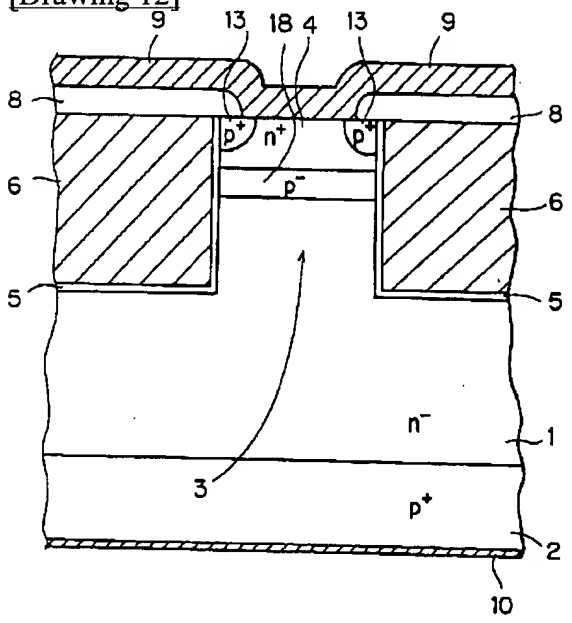
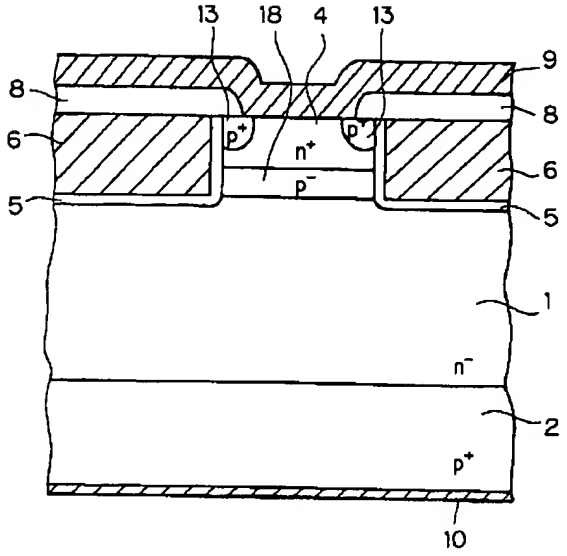



[Drawing 13]

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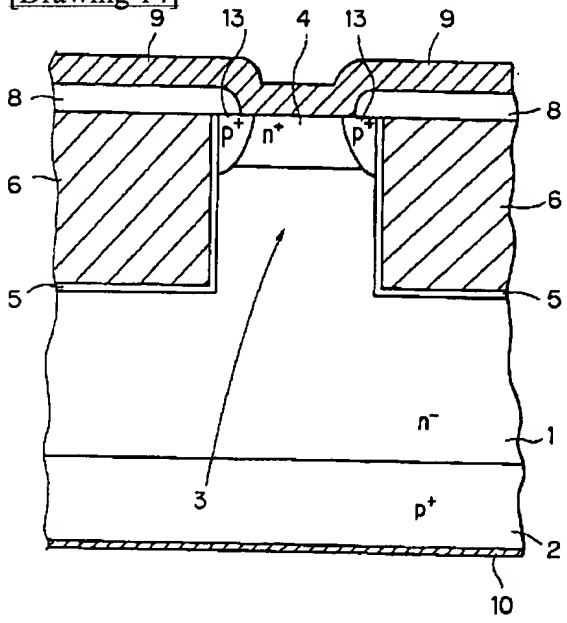


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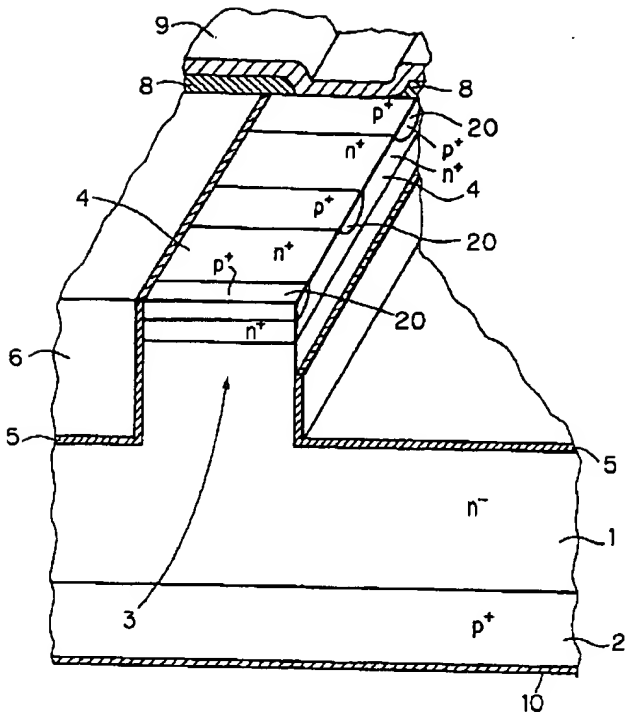


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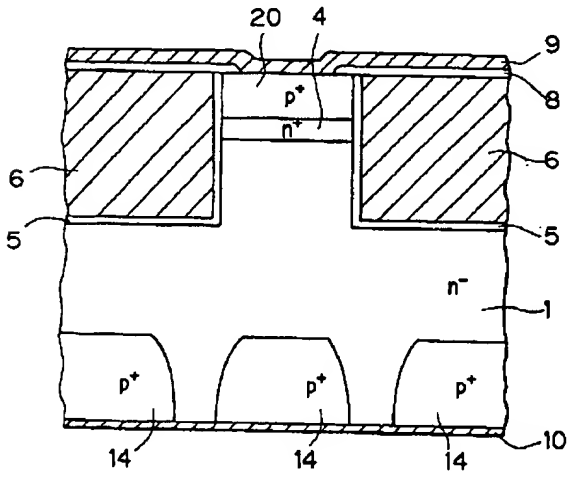


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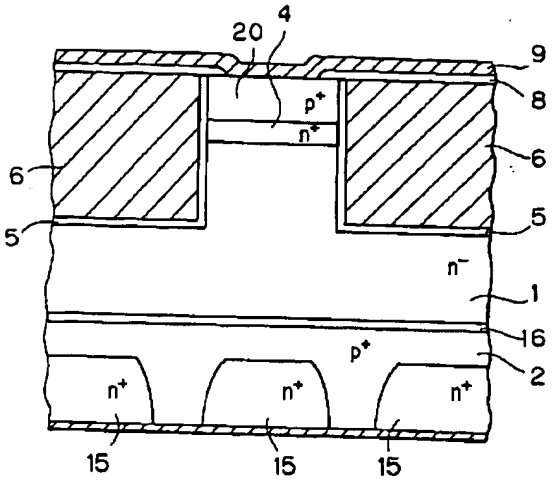
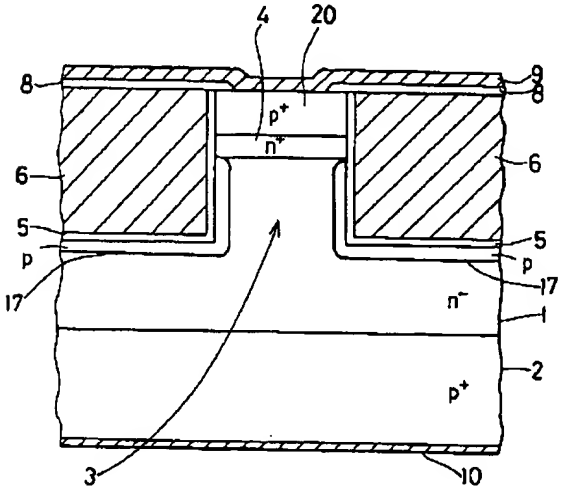



[Drawing 19]

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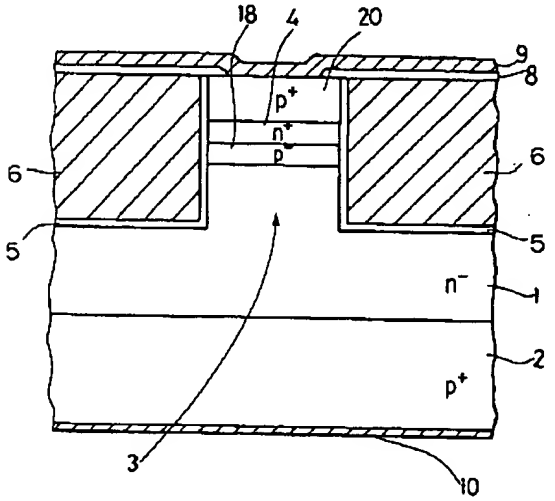


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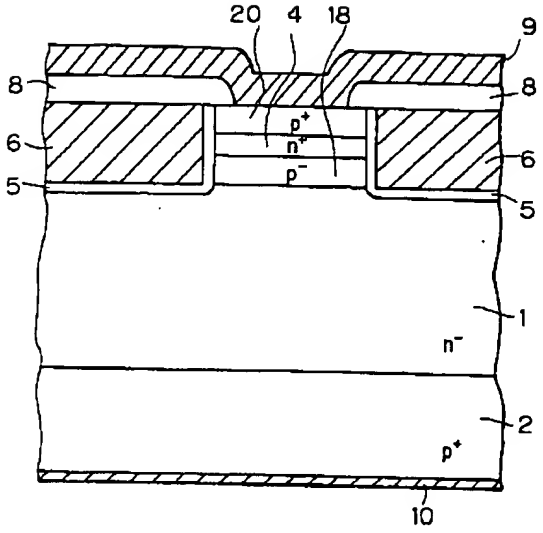


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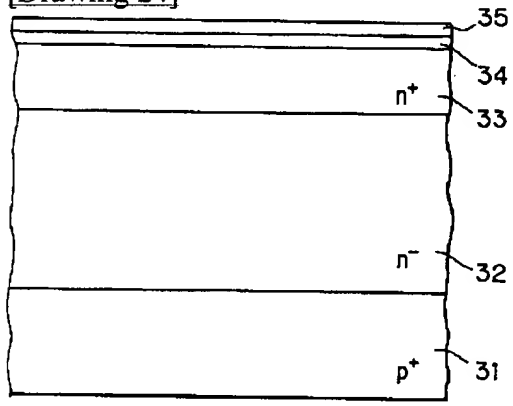


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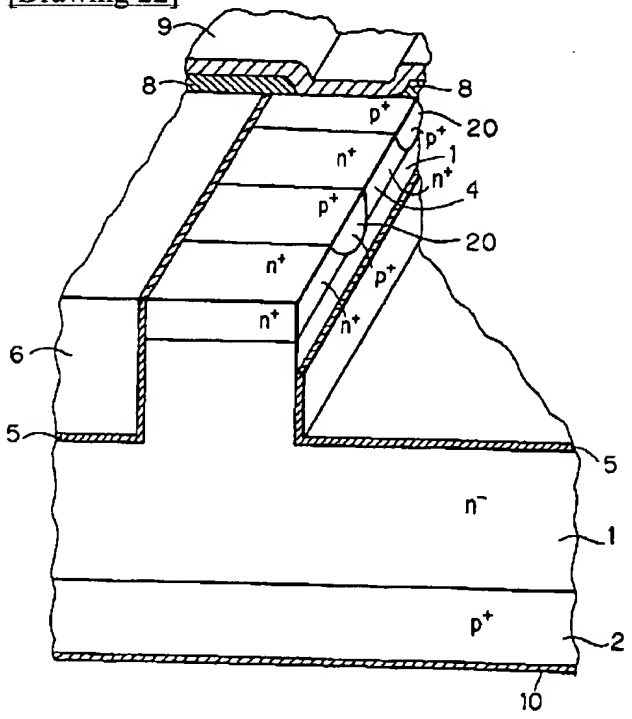
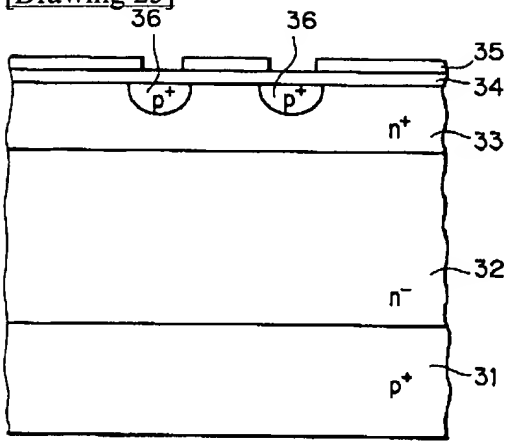
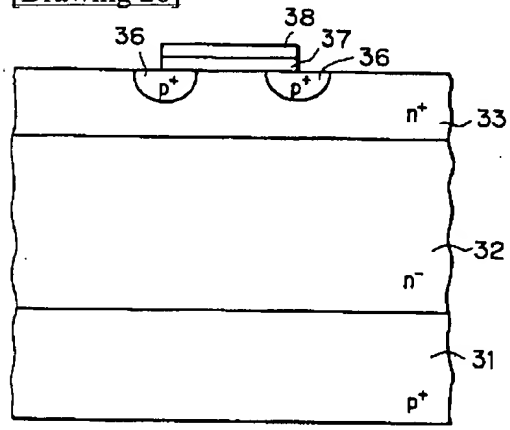


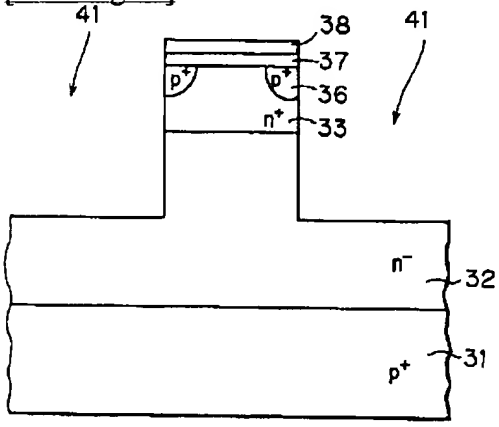
[Drawing 25]



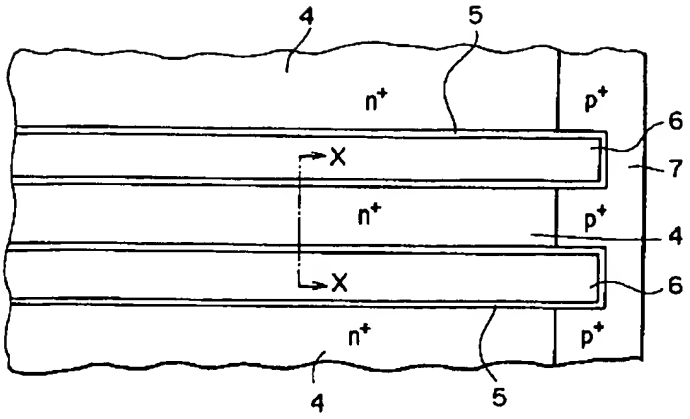

[Drawing 26]




[Drawing 27]




[Drawing 30]

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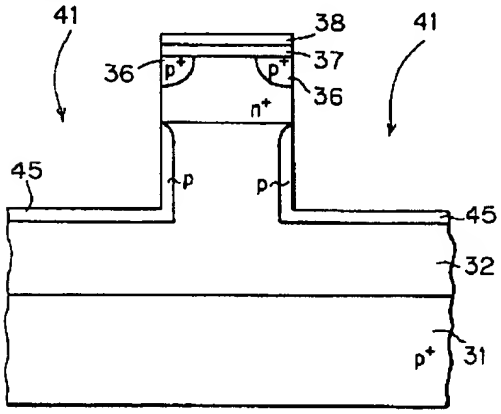


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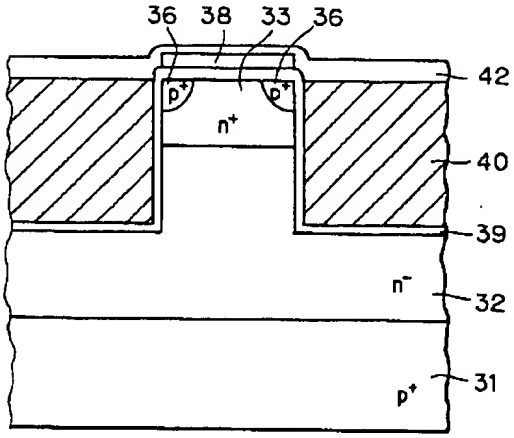


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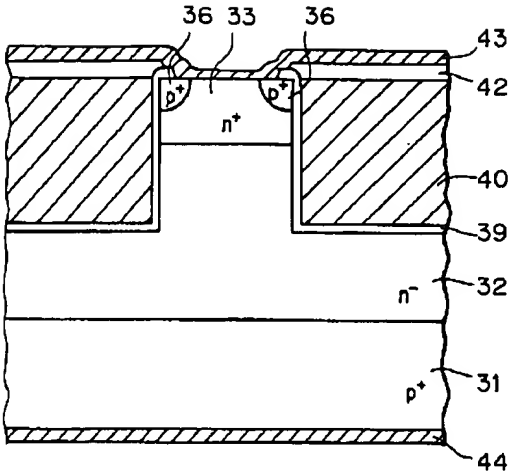


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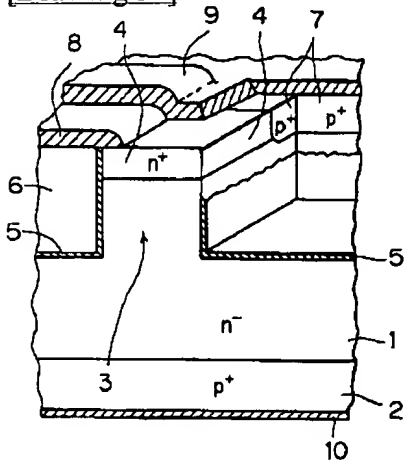


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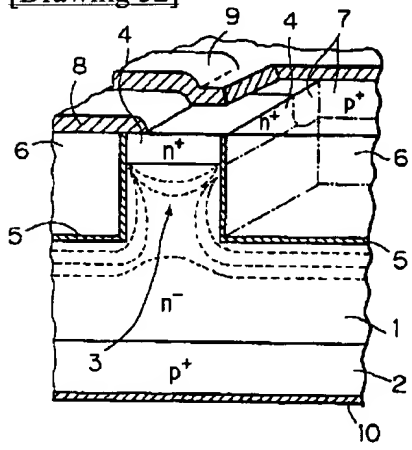


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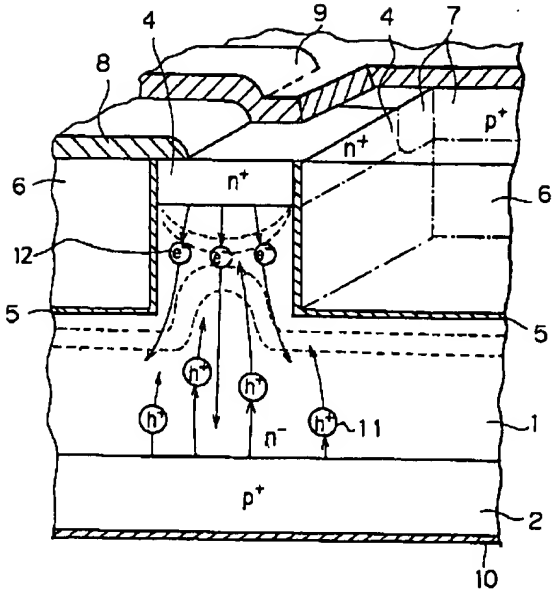
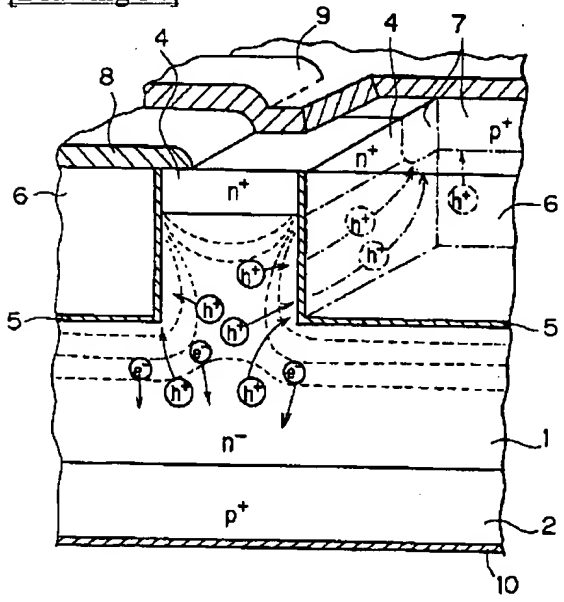



[Drawing 34]

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[Translation done.]